

CLAIMS

1. A differential charge pump comprising:
 - a capacitive structure having a first plate and a second plate;
 - a first control branch for charging the first plate when a first signal is asserted, and discharging the first plate when a second signal is asserted;
 - a second control branch for discharging the second plate when the first signal is asserted, and charging the second plate when the second signal is asserted;
 - a first common mode branch for charging or discharging the first plate to a common mode voltage when the first signal and the second signal are at the same level; and
 - a second common mode branch for charging or discharging the second plate to the common mode voltage when the first signal and the second signal are at the same level.
2. The differential charge pump of Claim 1, wherein the first common mode branch comprises a first transistor coupled between a first supply voltage and the first plate, wherein the second common mode branch comprises a second transistor coupled between the first supply voltage and the second plate, and wherein the differential charge pump further comprises a voltage control circuit for supplying a first gate voltage to a gate of the first transistor and second gate voltage to a gate voltage of the second transistor, the first gate voltage causing the first transistor to provide the common mode voltage to the first plate, and the second gate voltage causing the second transistor to provide the common mode voltage to the second plate.

3. The differential charge pump of Claim 2, wherein the voltage control circuit comprises:

an operational amplifier (op-amp); and
a third transistor coupled between the first supply voltage and a first input of the op-amp, wherein a gate of the third transistor is connected to the gate of the first transistor, the gate of the second transistor, and an output of the op-amp, and wherein a second input of the op-amp is coupled to receive the common mode voltage.

4. The differential charge pump of Claim 3, wherein the first transistor, the second transistor, and the third transistor are PMOS transistors,

wherein the first input of the op-amp is a non-inverting input, and

wherein the second input of the op-amp is an inverting input.

5. The differential charge pump of Claim 3, wherein the first transistor, the second transistor, and the third transistor are NMOS transistors,

wherein the first input of the op-amp is an inverting input, and

wherein the second input of the op-amp is a non-inverting input.

6. The differential charge pump of Claim 3, wherein the first common mode branch further comprises a fourth transistor coupled between the first plate and a second supply voltage,

wherein the second common mode branch further comprises a fifth transistor coupled between the second plate and the second supply voltage, and

wherein the differential charge pump further comprises a bias current control circuit for gate-biasing the fourth transistor and the fifth transistor as current sources for a bias current.

7. The differential charge pump of Claim 6, wherein the bias current control circuit comprises:

a sixth transistor; and

a seventh transistor coupled to receive the bias current, wherein the seventh transistor is gate-drain coupled, and wherein a gate of the seventh transistor is connected to the gate of the fourth transistor, a gate of the fifth transistor, and a gate of the sixth transistor.

8. The differential charge pump of Claim 7, wherein the first transistor, the second transistor, and the third transistor are coupled to the first supply voltage by a first constant-on switch, a second constant-on switch, and a third constant-on switch, respectively, and

wherein the fourth transistor, the fifth transistor, the sixth transistor, and the seventh transistor are coupled to the second supply voltage by a fourth constant-on switch, a fifth constant-on switch, a sixth constant-on switch, and a seventh constant-on switch, respectively.

9. The differential charge pump of Claim 8, wherein the first transistor, the second transistor, and the third transistor are matched, and wherein the fourth transistor, the

fifth transistor, the sixth transistor, and the seventh transistor are matched.

10. The differential charge pump of Claim 8, wherein the first control branch comprises a first current source coupled between the first supply voltage and the first plate by a first controllable switch and a second current source coupled between the first plate and the second supply voltage by a second controllable switch, and

wherein the first control branch comprises a third current source coupled between the first supply voltage and the second plate by a third controllable switch and a fourth current source coupled between the second plate and the second supply voltage by a fourth controllable switch,

wherein the first controllable switch and the fourth controllable switch close when the first signal is asserted, and

wherein the second controllable switch and the third controllable switch close when the second signal is asserted.

11. The differential charge pump of Claim 10, wherein the first transistor, the second transistor, the third transistor, the first current source, and the third current source are matched transistors,

wherein the fourth transistor, the fifth transistor, the sixth transistor, the seventh transistor, the second current source, and the fourth current source are matched transistors,

wherein the first constant-on switch, the second constant-on switch, the third constant-on switch, the first controllable switch, and the third controllable switch are matched transistors, and

wherein the fourth constant-on switch, the fifth constant-on switch, the sixth constant-on switch, the seventh constant-on

switch, the second controllable switch, and the fourth controllable switch are matched transistors.

12. A method for operating a differential charge pump, the method comprising:

providing a charging capacitor having a first plate and a second plate, the first plate being separated from the second plate by a dielectric;

charging the first plate and discharging the second plate when a first signal is asserted and a second signal is deasserted;

charging the second plate and discharging the first plate when the first signal is deasserted and the second signal is asserted; and

driving the first plate and the second plate to a common mode voltage when the first signal and the second signal are at the same level.

13. The method of claim 12, wherein driving the first plate and the second plate to the common mode voltage comprises:

supplying a first gate voltage to a first transistor coupled between a first supply voltage and the first plate and a second transistor coupled between the first supply voltage and the second plate, wherein the first gate voltage causing the first transistor and the second transistor to provide the common mode voltage to the first plate and the second plate, respectively;

supplying a second gate voltage to a third transistor coupled between the first plate and a second supply voltage and a fourth transistor coupled between the second plate and the second supply voltage, the second gate voltage causing the third transistor and the fourth transistor to source a bias current.

14. The method of Claim 13, wherein supplying the first gate voltage comprises supplying the common mode voltage to a first input of an operational amplifier (op-amp),

wherein an output of the op-amp is coupled to a gate of a fifth transistor, the fifth transistor being coupled between the first supply voltage and a second input of the op-amp, and

wherein the gate of the fifth transistor is coupled to a gate of the first transistor and a gate of the second transistor.

15. The method of Claim 14, wherein the first transistor, the second transistor, and the fifth transistor are PMOS transistors,

wherein the first input of the op-amp is an inverting input, and

wherein the second input of the op-amp is a non-inverting input.

16. The method of Claim 14, wherein the first transistor, the second transistor, and the fifth transistor are NMOS transistors,

wherein the first input of the op-amp is a non-inverting input, and

wherein the second input of the op-amp is an inverting input.

17. The method of Claim 14, wherein supplying the second gate voltage comprises supplying the bias current to a sixth transistor, the sixth transistor being gate-drain coupled,

wherein a gate of the sixth transistor is coupled to a gate of a seventh transistor, the seventh transistor being coupled between the fifth transistor and the second supply voltage, and

wherein the gate of the seventh transistor is coupled to a gate of the third transistor and a gate of the fourth transistor.

18. A differential charge pump comprising:

a first control branch coupled between a first supply voltage and a second supply voltage;

a second control branch coupled between the first supply voltage and the second supply voltage;

a capacitive structure coupled between the first control branch and the second control branch;

a first transistor coupled between the first supply voltage and a first plate of the capacitive structure;

a second transistor coupled between the first supply voltage and a second plate of the capacitive structure;

a third transistor, wherein a gate of the third transistor is connected to a gate of the first transistor and a gate of the second transistor; and

a voltage control circuit for regulating a first gate voltage at the gate of the third transistor to cause the third transistor to output a common mode voltage.

19. The differential charge pump of Claim 18, wherein the voltage control circuit comprises an operational amplifier (op-amp), wherein the third transistor is coupled between the first supply voltage and a first input of the op-amp,

wherein an output of the op-amp is coupled to the gate of the third transistor, and

wherein a second input of the op-amp is coupled to receive the common mode voltage.

20. The differential charge pump of Claim 19, wherein the third transistor is a PMOS transistor,

wherein the first input of the op-amp is a non-inverting input, and

wherein the second input of the op-amp is an inverting input.

21. The differential charge pump of Claim 19, wherein the third transistor is an NMOS transistor,

wherein the first input of the op-amp is an inverting input, and

wherein the second input of the op-amp is a non-inverting input.

22. The differential charge pump of Claim 19, wherein the common mode voltage is half of the first supply voltage.

23. The differential charge pump of Claim 18, further comprising:

a fourth transistor coupled between the first plate and the second supply voltage;

a fifth transistor coupled between the second plate and the second supply voltage;

a sixth transistor coupled between the third transistor and the second supply voltage, wherein a gate of the sixth transistor is coupled to a gate of the fourth transistor and a gate of the fifth transistor; and

a current control circuit for providing a second gate voltage to the sixth transistor to cause the sixth transistor to source a bias current.

24. The differential charge pump of Claim 23, wherein the current control circuit comprises a seventh transistor coupled to receive the bias current, wherein the seventh transistor is gate-drain coupled, and wherein a gate of the seventh transistor is coupled to the gate of the sixth transistor.

25. The differential charge pump of Claim 24, wherein the first transistor, the second transistor, and the third transistor are matched transistors, and

wherein the fourth transistor, the fifth transistor, the sixth transistor, and the seventh transistor are matched transistors.

26. The differential charge pump of Claim 24, wherein the first transistor, the second transistor, and the third transistor are coupled to the first supply voltage by a first constant-on switch, a second constant-on switch, and a constant-on third switch, respectively, and

wherein the fourth transistor, the fifth transistor, the sixth transistor, and the seventh transistor are connected to a second supply voltage by a fourth constant-on switch, a fifth constant-on switch, a sixth constant-on switch, and a seventh constant-on switch, respectively.

27. The differential charge pump of Claim 26, wherein the first transistor, the second transistor, and the third transistor are matched transistors,

wherein the first constant-on switch, the second constant-on switch, and the constant-on third switch are matched transistors,

wherein the fourth transistor, the fifth transistor, the sixth transistor, and the seventh transistor are matched transistors, and

wherein the fourth constant-on switch, the fifth constant-on switch, the sixth constant-on switch, and the seventh constant-on switch are matched transistors.

28. The differential charge pump of Claim 19, wherein the first plate and the second plate form a first capacitor, and

wherein the capacitive structure further comprises a third plate and a fourth plate forming a second capacitor, the third plate being connected to the first plate, and the fourth plate being connected to the second plate,

wherein the first plate and the fourth plate are formed in a first metal layer, and

wherein the second plate and the third plate are formed in a second metal layer.